SPECIFICATION AMENDMENTS

Page 8, please change the paragraph spanning lines 11-21 to read as follows:

Fig. 2 schematically illustrates the potential distribution along a line A-A' in Fig. 1. There are shown electrons 20 constituting carriers; the gate insulation film 22 and the insulating substrate 21. The important features of the present invention are that (1) the carrier electrons drift in an area separate from the interface between the gate insulation film 22 and the semiconductor, (2) the drifting area of the carriers 20 has a gentle slope of electric field toward the gate surface, and (3) the carrier drift area has a low impurity concentration.

Pages 9 and 10, please change the paragraph bridging pages 9 and 10 to read as follows:

The p^+-area 4 of high impurity concentration at the surface needs to have a thickness at least equal to the mean free path of drifting carriers, in order to reduce the probability of scattering at the interface with the gate insulation film. More specifically, in case of silicon, said thickness is preferably selected equal to 50 - 100 Å or larger. The impurity concentration is preferably higher, by one digit or more, than that in the area 3. The semiconductor layer may be depleted to the interface between the semiconductor and the gate insulation film, or may remain neutral. Fig. 2 shows the former state. The carrier

induction under the application of a voltage to the gate electrode should preferably take place, but in the area 3. In case of an n-area, free carriers can be easily generated in the area 3 if the Fermi level is above the center of the forbidden band. In case of a p-area, there is required a level of $-2\phi_F$ opposite to the inherent Fermi level ϕ_F in order to generate electrons which are of the opposite conductive type.